1. A thin film semiconductor die package structure comprising :

one or more semiconductor dies backside bonded on planar glass substrate;

one or more layers of interconnect metal connected to and above said semiconductor dies; and

one or more insulating layers of polymer with contact holes, formed around said interconnect metal.

2. The thin film semiconductor package structure of claim 1 wherein the substrate is diced into single chip semiconductor packages.

3. The thin film semiconductor package structure of claim 1 wherein the substrate is diced into multi-chip semiconductor packages.

4. The thin film semiconductor package of claim 3 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise the same type of integrated circuit chips.

5. The thin semiconductor package of claim 3 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise different types of integrated circuit chips.

6. The thin film semiconductor package structure of claim 1 wherein solder bumps are connected to said interconnect metal and incorporated as interconnects to the next level of assembly.

7. The thin film semiconductor package structure of claim 1 incorporating connector pins connected to said interconnect metal and for assembly to the next level of packaging.

8. The thin film semiconductor package structure of claim 1 wherein said one or more layers of interconnect metal and said one or more insulating layers comprise an interconnect system, and wherein one or more devices are incorporated within said interconnect system.

9. The thin film semiconductor package structure of claim 8 wherein said one or more devices are selected from the group comprising inductors, resistors, capacitors, waveguides, filters and MEMS devices.

10. A thin film semiconductor die packaging structure comprising:

one or more semiconductor dies backside bonded on a planar glass substrate, wherein the glass substrate has cavities on the top surface for containing and bonding the semiconductor dies;

one or more layers of interconnect metal connected to and above said semiconductor dies; and

one or more insulating layers of polymer with contact holes, formed around said interconnect metal.

11. The thin film semiconductor package structure of claim 1 further comprising epoxy on said glass substrate and adjacent to said one or more semiconductor dies.

12. The thin film semiconductor package structure of claim 10 wherein the substrate is diced into single semiconductor die packages.

13. The thin film semiconductor package structure of claim 10 wherein the substrate is diced into multi-chip semiconductor packages.

14. The thin film semiconductor package of claim 10 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise the same type of integrated circuit chips.

15. The thin semiconductor package of claim 10 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise different types of integrated circuit chips.

16. The thin film semiconductor package structure of claim 10 wherein one or more solder bumps are incorporated for interconnect to the next level of assembly.

17. The thin film semiconductor package structure of claim 10 wherein one or more connector pins are incorporated for interconnect to the next level of assembly.

18. The thin film semiconductor package structure of claim 10 wherein said one or more layers of interconnect metal and said one or more insulating layers comprise an interconnect system, and wherein one or more devices are incorporated within said interconnect system.

19. The thin film semiconductor package structure of claim 17 wherein said one or more devices are selected from the group comprising inductors, resistors, capacitors, waveguides, filters and MEMS devices.

20. A thin film semiconductor die packaging structure comprising :

one or more semiconductor dies backside bonded on a metal-glass composite substrate, wherein the glass has cavities for containing and bonding the semiconductor dies;

one or more layers of interconnect metal connected to and above said semiconductor dies; and

one or more insulating layers of polymer with contact holes, formed around said interconnect metal.

21. The thin film semiconductor package structure of claim 20 wherein the substrate is diced into single semiconductor die packages.

22. The thin film semiconductor package structure of claim 20 wherein the substrate is diced into multi-chip semiconductor die packages.

23. The thin film semiconductor package of claim 22 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise the same type of integrated circuit chips.

24. The thin semiconductor package of claim 22 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise different types of integrated circuit chips.

25. The thin film semiconductor package structure of claim 20 wherein one or more solder bumps are incorporated for interconnection to the next level of assembly.

26. The thin film semiconductor package structure of claim 20 wherein one or more connector pins are incorporated for interconnecting to the next level of assembly.

27. The thin film semiconductor package structure of claim 20 wherein said one or more layers of interconnect metal and said one or more insulating layers comprise an interconnect system, and wherein one or more devices are incorporated within said interconnect system.

28. The thin film semiconductor package structure of claim 20 wherein said one or more devices are selected from the group comprising inductors, resistors, capacitors, waveguides, filters and MEMS devices.

29. A thin film semiconductor die packaging structure comprising :

one or more semiconductor dies backside bonded on a glass substrate;

one or more layers of interconnect metal connected to and above said semiconductor dies;

a glass layer between said semiconductor dies and the first of said one or more layers of interconnect metal; and

one or more insulating layers of polymer with contact holes, formed around said interconnect metal.

30. The thin film semiconductor package structure of claim 29 wherein the substrate is diced into single semiconductor die packages.

31. The thin film semiconductor package structure of claim 29 wherein the substrate is diced into multi-chip semiconductor die packages.

32. The thin film semiconductor package of claim 31 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise the same type of integrated circuit chips.

33. The thin semiconductor package of claim 31 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise different types of integrated circuit chips

34. The thin film semiconductor package structure of claim 29 wherein one or more solder bumps are incorporated for interconnection to the next level of assembly.

35. The thin film semiconductor package structure of claim 29 wherein one or more connector pins are incorporated for interconnecting to the next level of assembly.

36. The thin film semiconductor package structure of claim 29 wherein said one or more layers of interconnect metal and said one or more insulating layers comprise an interconnect system, and wherein one or more devices are incorporated within said interconnect system.

37. The thin film semiconductor package structure of claim 29 wherein said one or more devices are selected from the group comprising inductors, resistors, capacitors, waveguides, filters and MEMS devices.

38. The thin film semiconductor package structure of claim 29 further comprising epoxy formed on said glass substrate and between said semiconductor dies.

39. A method for fabricating a thin film semiconductor die package, comprising the steps of:

providing a planar glass substrate;

attaching semiconductor dies to said planar glass substrate;

sequentially depositing one or more polymer layers and one or more metal interconnect layers over said substrate;

forming a layer of solder over and connected to said one or more metal interconnect layers; and

reflowing the solder to form solder bumps.

40. A method of fabricating a thin film semiconductor die package structure comprising the steps of :

providing a glass substrate with cavities having semiconductor dies mounted therein;

sequentially forming polymer insulating layers and metal interconnect layers;

forming a layer of solder; and

reflowing the solder to form solder bumps.

41. A method of fabricating the thin film semiconductor die package structure comprising:

providing a metal substrate;

forming a glass layer with cavities for mounting semiconductor dies on said metal substrate;

sequentially forming polymer insulating layers and metal interconnect layers;

forming a layer of solder; and

reflowing the solder to form solder bumps

42. A method of fabricating a thin film semiconductor die package structure comprising:

providing a glass substrate with semiconductor dies mounted on the active surface;

filling polymer or epoxy between and over the backside of said semiconductor dies, to obtain a planarized surface;

grinding the planarized surface, and said backside of said semiconductor dies, to a desired thickness of said semiconductor dies;

mounting a second glass substrate on the backside of the semiconductor dies;

grinding the first glass substrate to a desired glass thickness;

etching holes in said first glass substrate to expose said semiconductor dies;

sequentially forming polymer insulating layers and metal interconnect layers over said first glass substrate;

depositing a layer of solder; and

reflowing the solder to form solder bumps.

43. The method of claim 42 wherein said desired thickness of said semiconductor dies is between about 2 and 500 um.

44. The method of claim 42 wherein said desired glass thickness is between about 2 and 150 um.

45. The method of claim 42 further comprising dicing said thin film semiconductor die package structure into single chip semiconductor packages.

46. The method of claim 42 further comprising dicing said thin film semiconductor die package structure into multi-chip semiconductor packages.

47 The method of claim 46 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise the same type of integrated circuit chips.

48. The method of claim 46 wherein said semiconductor dies mounted within said multi-chip semiconductor packages comprise different types of integrated circuit chips

49. The method of claim 42 wherein solder bumps are connected to said interconnect metal and incorporated as interconnects to the next level of assembly.

50. The method of claim 42 wherein connector pins are connected to said interconnect metal and for assembly to the next level of packaging.

51. The method of claim 42 wherein said one or more layers of interconnect metal and said one or more insulating layers comprise an interconnect system, and further comprising incorporating one or more devices within said interconnect system.

52. The method of claim 51 wherein said one or more devices are selected from the group comprising inductors, resistors, capacitors, waveguides, filters and MEMS devices.

53. A method of fabricating a thin film semiconductor die package structure comprising:

providing a glass substrate with semiconductor dies mounted on the active surface;

filling polymer or epoxy between and over the backside of said semiconductor dies, to obtain a planarized surface;

grinding the planarized surface, and said backside of said semiconductor dies, to a desired thickness of said semiconductor dies;

mounting a second glass substrate on the backside of the semiconductor dies;

removing said first glass substrate;

sequentially forming polymer insulating layers and metal interconnect layers over said semiconductor dies;

depositing a layer of solder; and

reflowing the solder to form solder bumps.

54. The thin film semiconductor die package structure of claim 1 wherein said one or more layers of interconnect metal are used as interconnections between one or more points of electrical contact on each of said semiconductor dies.

55. The thin film semiconductor die package structure of claim 10 wherein said one or more layers of interconnect metal are used as interconnections between one or more points of electrical contact on each of said semiconductor dies.

56. The thin film semiconductor die package structure of claim 20 wherein said one or more layers of interconnect metal are used as interconnections between one or more points of electrical contact on each of said semiconductor dies.

57. The method of claim 42 further comprising using said one or more layers of interconnect metal for interconnections between one or more points of electrical contact on each of said semiconductor dies.

58. The method of claim 53 further comprising using said one or more layers of interconnect metal for interconnections between one or more points of electrical contact on each of said semiconductor dies.